PULSUS
Future of Digital Audio

PS8536 Datasheet (Ver0.96)

USB Streaming Audio Processor with 5Wx2 Speaker Amplifier

2011-06-20

High-Fidelity Full-Digital Amplifier for USB Speakers

USB Streaming Audio Processor with 5Wx2 Speaker Amplifier

Introduction

PS8536 is a highly integrated system-on-chip solution for USB speaker applications. It combines all essential active parts including USB interface, a high-performance stereo PWM modulator, a sophisticated sample rate converter, a stereo speaker amplifier and state-of-art digital signal processing.

Built-in USB interface supports both 5V power supply and adaptive isochronous transfer for playback. On-chip full-digital stereo speaker amplifier is rated at 5-watt per channel with 96% efficiency under the external power source, 6.6V

PS8536 fully supports sound processing including five-band equalizer, dynamic range control (DRC), mute, volume, and auto gain limiter. The equalizer setting may be selected from a large set of preset equalizer pool optimized for the most popular speakers in the market. With PS8536, you could easily apply the button controls for bass, treble, dynamic range control, volume and mute controls.

Through the on-chip I^2S interface, the PS8536 may also receive additional digital sources. I^2C control bus and GPIO allows full compatibility and easy configuration.

Advantages

- ✓ Outstanding sound quality from patented full digital amplifier.
- ✓ No additional active components for USB speakers required.
- ✓ Sophisticated on-chip sample rate converter.
- ✓ Sound processing: equalizer, bass, treble, DRC, etc.
- ✓ Easy speaker tuning and user sound effects control
- ✓ Supports selectable optimized speaker tuning for both 4Ω and 8Ω speakers

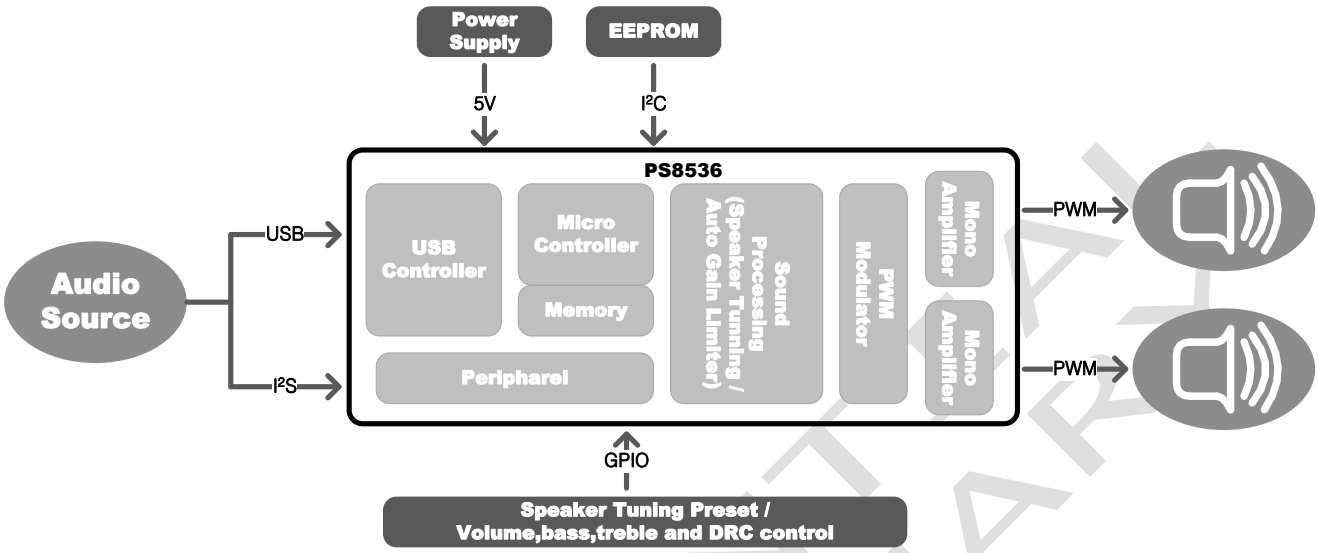
Features

- ✓ High Output Power
  - ■ USB bus powered
    1.1Wx2 @5V, 4Ω, THD+N 10%
  - ■ External powered
    4.5Wx2 @6.6V, 4Ω, THD+N 10%
    2.6Wx2 @5.0V, 4Ω, THD+N 10%
- ✓ On-chip USB interface
  - ■ USB1.1 specification full-speed compatible
  - ■ No required device driver
  - ■ Adaptive isochronous transfer for playback
- ✓ Windows 98/XP/Vista, Mac OS and Linux compatible
- ✓ Multiple functions
  - ■ GPIO (general purpose inputs and outputs)
  - ■ Stereo serial input ports(I^2S)
  - ■ I^2C control bus
- ✓ Audio source select using a pin : USB/I^2S
- ✓ High-performance digital to digital converter
- ✓ Independently adaptive sample rate : up to 96kHz
- ✓ On-chip sample rate converter
- ✓ Clipping free processing with on-chip DRC
- ✓ 5-band full parametric equalizer for channel
- ✓ Digital volume control and DRC control
- ✓ Soft volume adjustment & soft mute control
- ✓ Click noise free
- ✓ Easy speaker tuning by preset equalizer with GPIO
- ✓ Equalizer and filter value setting available with EEPROM
- ✓ GPIO controlled bass, treble, DRC, volume & mute
- ✓ Embedded clock generator (PLL)
- ✓ Vendor-identification, PID, String available with external EEPROM
- ✓ Over-heat protection
- ✓ UVP(Under voltage protection)
- ✓ OCP(Over current protection)
- ✓ SCP(Short circuit protection)
- ✓ 56-Lead QFN 7x7

Applications

- ✓ USB PC speakers
- ✓ USB monitors
- ✓ USB connection consumer audio devices

Block Diagram



REMARK

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this datasheet may have changed since this data sheet was published.
3. Pulsus Technologies, Inc. reserves the right to make changes in the products – including circuits, standard cells, and/or software described or contained herein in order to improve design and/or performance.

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Contents

1 ELECTRICAL SPECIFICATIONS

1.1 Absolute Maximum Ratings

Power Supply Voltage Range, VDD50.....-0.5V to 5.5V
Power Supply Voltage Range, PVDD50.....-0.3V to 7.0V
Power Supply Voltage Range, VDD33.....-0.5V to 4.0V
Power Supply Voltage Range, VDD18.....-0.5V to 2.1V
Digital Input Voltage.....-0.5V to 4.0V
Storage Temperature.....-0.5°C to +150°C
Operating Temperature.....-0.5°C to +125°C

※ Stresses exceeding absolute maximum ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1.2 Recommended Operating Conditions

Recommended Operating Conditions						
PARAMETERS		SYMBOL	MIN.	TYP.	MAX.	UNITS
DC Power Supply	USB Power	VDD50	3.30		5.00	V
	I/O Power	VDD33	2.97	3.30	3.63	V
	Core Power	VDD18	1.62	1.80	1.98	V
	PLL Power	AVDD18	1.62	1.80	1.98	V
	BTL Power	PVDD50	2.70	5.00	6.60	V
Ground		PGND, Ground PAD		0		V
DC Power Supply	USB Power	VDD50		TBD		mA
	I/O Power	VDD33		TBD		mA
	Core Power	VDD18		TBD		mA
	PLL Power	AVDD18		TBD		mA
	BTL Power	PVDD50		TBD		mA
Ambient Operating Temperature				TBD		°C

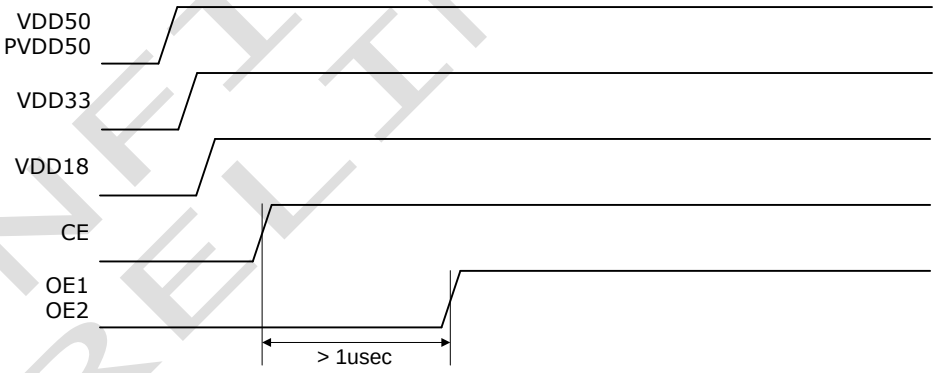
1.3 Audio Electrical Characteristics

Audio Electrical Characteristics					
PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS
Speaker Output Power (Stereo)	SPKOUT				
External power 5.0V, THD+N ≤ 10%, 4Ω				2.63	W
External power 6.6V, THD+N ≤ 10%, 4Ω				4.50	W

1.4 Digital Electrical Characteristics

PARAMETERS		SYMBOL	MIN.	TYP.	MAX.	UNITS
Input Leakage Current		IL	-10		+10	μA
Tri-State Output Leakage Current		IOZ	-10		+10	μA
High-level Input Voltage	Normal Input	VIH	2.00		5.50	V
	Schmitt Input	VT+	1.40	1.50	1.59	V
Low-level Input Voltage	Normal Input	VIL	-0.30		0.80	V
	Schmitt Input	VT-	0.88	0.94	1.00	V
Schmitt Threshold Point		VT	1.35	1.47	1.60	V
Pull-down Resistance		RPD	43k	55k	97k	Ω
Pull-up Resistance		RPU	46k	66k	97k	Ω
Output Low Voltage		VOL			0.4	V
Output High Voltage		VOH		5		V

1.5 Power up sequence



1.6 Switching Characteristics – I^2S

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNITS
Data Hold Time	$T_{HDIS(I^2S)}$	50			ns
Data Setup Time	$T_{SUIS(I^2S)}$	50			ns
Clock High Time	$T_{HIGH(I^2S)}$	160	360		ns
Clock Low Time	$T_{LOW(I^2S)}$	160	360		ns
Rising Time of MBCK,SBCK	$T_{RISS(I^2S)}$			40	ns
Rising Time of MBCK,SBCK	$T_{FISS(I^2S)}$			40	ns
Delay until Valid Data		40		80	ns

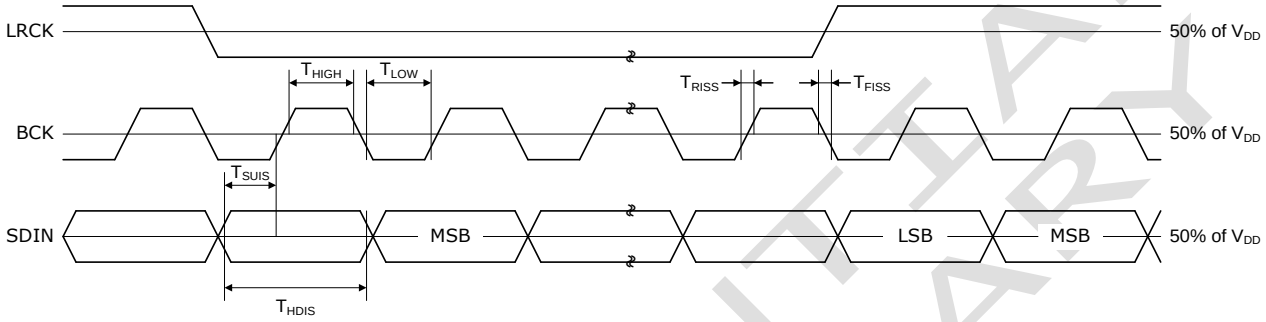


Figure 1-1 I^2S Timing

1.6 Switching Characteristics – I^2C

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNITS
SCL Clock Frequency				400	kHz
START (REPEAT) Condition Hold Time	$T_{HDST(I^2C)}$	400			ns
Low Period of SCL Clock	$T_{LOW(I^2C)}$	800			ns
High Period of SCL Clock	$T_{HIGH(I^2C)}$	800			ns
Setup Time for START REPEAT Condition	$T_{SUST(I^2C)}$	400			ns
Data Hold Time	$T_{HDD(I^2C)}$	0			ns
Data Setup Time	$T_{SUD(I^2C)}$	100			ns
Rise Time of both SDA and SCL	$T_{R(I^2C)}$			600	ns
Falling Time of both SDA and SCL	$T_{F(I^2C)}$			600	ns
Setup Time for STOP Condition	$T_{SUSP(I^2C)}$	400			ns
Bus Free Time between STOP and START Condition		470			ns

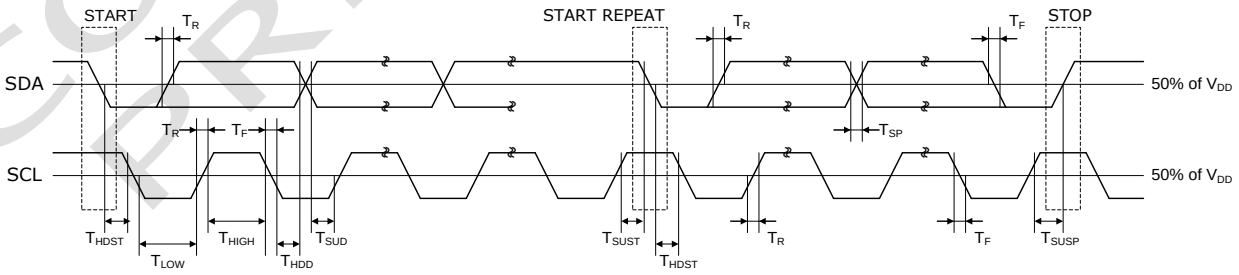


Figure 1-2 I^2C Timing

2 PIN INFORMATION

2.1 Pin Assignments

[TOP VIEW]

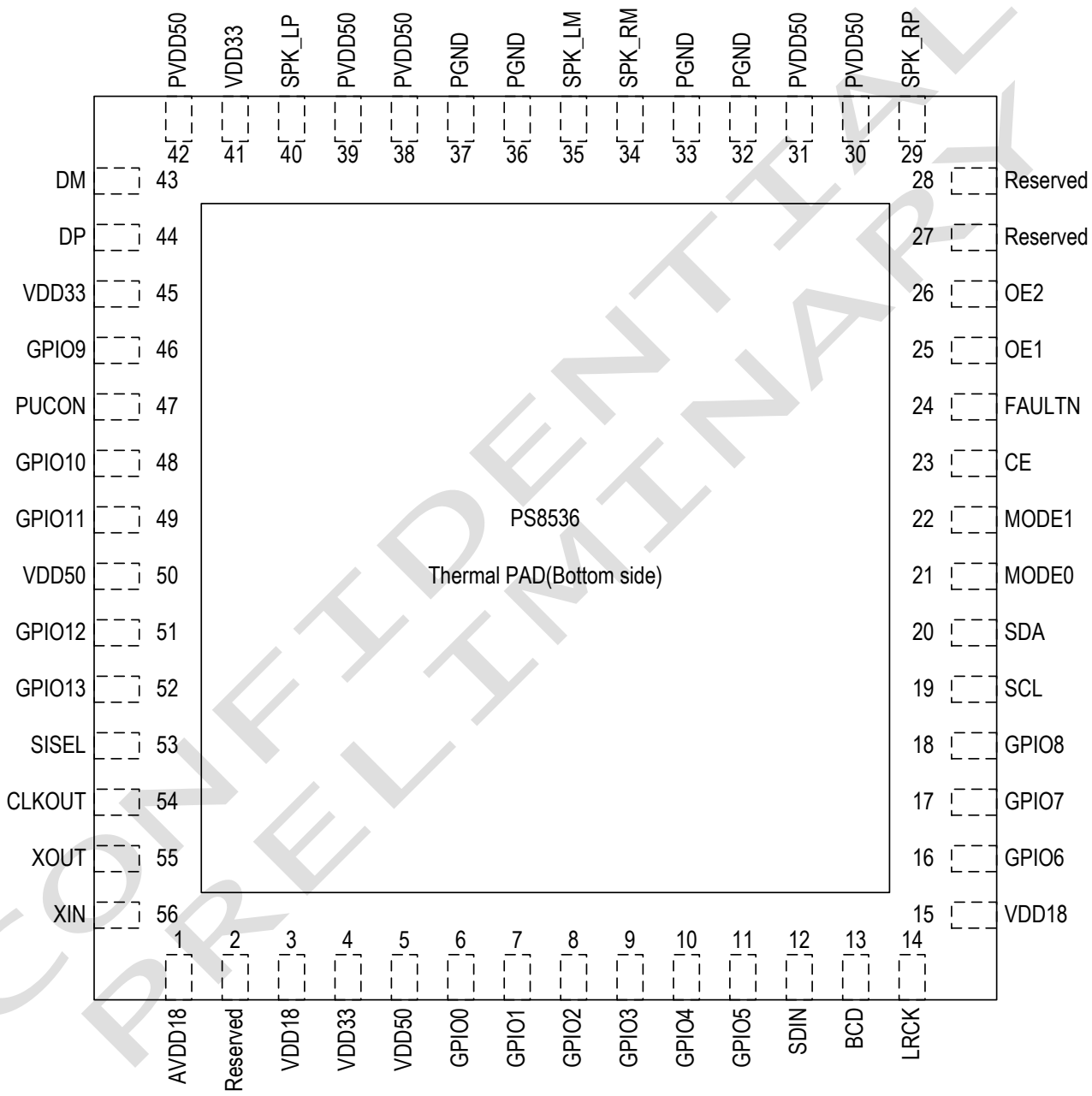


Figure 2-1 Pin Assignments

2.2 Pin description

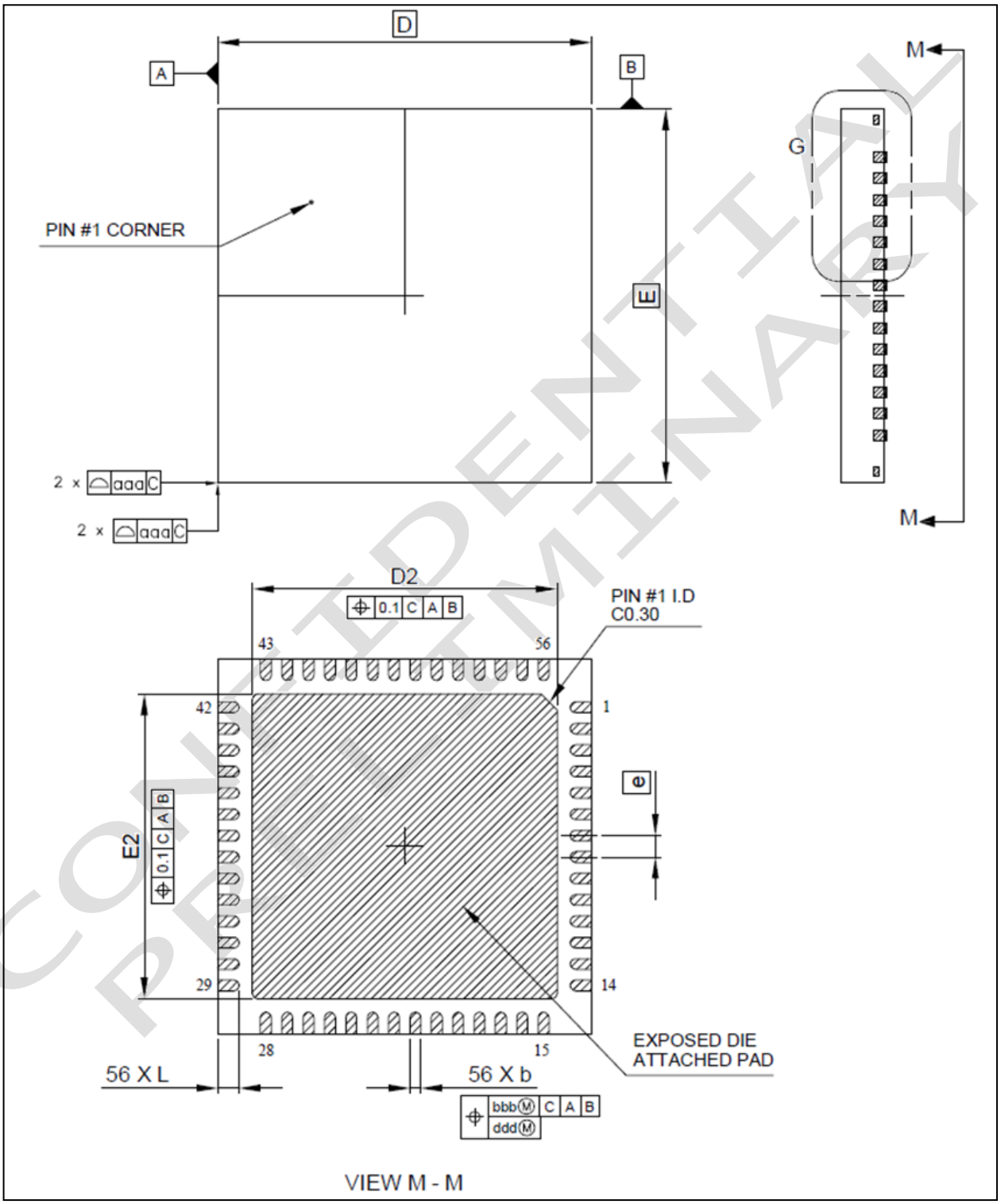
PIN NAME	PIN NO	TYPE	DESCRIPTION
POWER AND GROUND			
VDD33	4, 41, 45	Power	I/O power supply. 3.3V supply voltage.
VDD18(AVDD18)	3, 15, (1)	Power	(PLL) Logic power supply. 1.8V supply voltage.
VDD50	5, 50	Power	5V power supply.(Either USB or External or LDO)
PVDD50	30, 31, 38, 39, 42	Power	5V power supply
PGND	32, 33, 36, 37	Ground	Ground of power amplifier
GND_PAD	Bottom	Ground	Ground of all digital power.
USB INTERFACE			
DM	43	I/O	USB differential input/output minus.
DP	44	I/O	USB differential input/output plus.
SYSTEM SERVICES			
XIN	56	I	Crystal oscillator input.
XOUT	55	O	Crystal oscillator output.
CLKOUT	54	O	12MHz output.
SISEL	53	I/O	Audio source select(Pull-down) High:I2S, Low:US
PUCON	47	O	Boot on flag.
MODE0	21	I	Must be set low. (Pull-down)
MODE1	22	I	Must be set low. (Pull-down)
SYSTEM CONTROL INTERFACE			
SCL	19	I/O	I2C clock. (Pull-up)
SDA	20	I/O	I2C data. (Pull-up)
GENERAL PURPOSE INPUT/OUTPUT			
GPIO0	6	I/O	GPIO (Pull-up)
GPIO1	7	I/O	GPIO (Pull-up)
GPIO2	8	I/O	GPIO (Pull-up)
GPIO3	9	I/O	GPIO (Pull-up)
GPIO4	10	I/O	GPIO (Pull-up)
GPIO5	11	I/O	GPIO (Pull-up)
GPIO6	16	I/O	GPIO (Pull-up)
GPIO7	17	I/O	GPIO (Pull-up)
GPIO8	18	I/O	GPIO (Pull-up)
GPIO9	46	I/O	GPIO (Pull-up)
GPIO10	48	I/O	GPIO (Pull-up)
GPIO11	49	I/O	GPIO (Pull-up)
GPIO12	51	I/O	GPIO (Pull-up)
GPIO13	52	I/O	GPIO (Pull-up)
AUDIO INPUT/OUTPUT INTERFACE			
SDIN	12	I	PCM input serial data. (Pull-up)
BCK	13	I	PCM bit clock. (Pull-up)
LRCK	14	I	PCM word clock. (Pull-up)
OUTPUT STAGE			
CE	23	I	Chip enable for Power stage, Active high (Internal pull-down resistor 150kohm)
FAULTN	24	O	Fault Status Output. Active-Low Open-Drain Output (external pull-up)

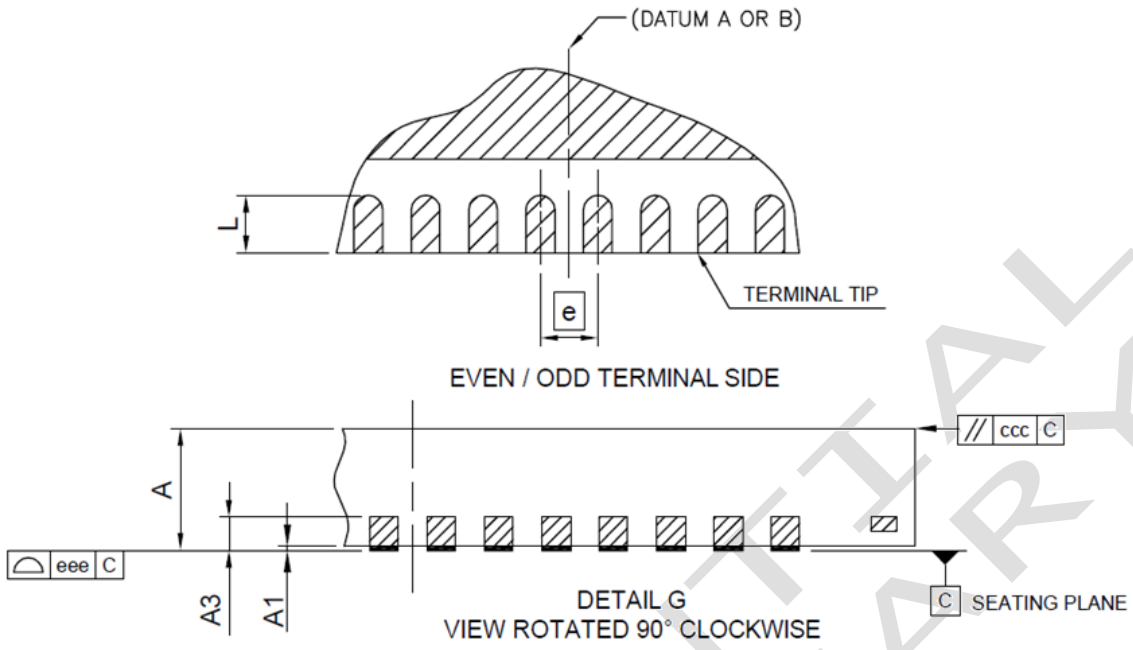
OE1	25	I	Output enable for SPK_L channel, Active high (Internal pull-down resistor 150kohm)
OE2	26	I	Output enable for SPK_R channel, Active high (Internal pull-down resistor 150kohm)
SPK_RP	29	Analog O	Positive BTL driver output of right channel PWM.
SPK_RM	34	Analog O	Negative BTL driver output of right channel PWM.
SPK_LP	40	Analog O	Positive BTL driver output of left channel PWM.
SPK_LM	35	Analog O	Negative BTL driver output of left channel PWM.
etc.			
Reserved	2	O	Reserved
Reserved	27,28	I/O	Reserved (Pull-up)

3 PACKAGE INFORMATION

3.1 Package Dimensions

(QFN, 7mm x 7mm, 56LD, 0.4mm Lead Pitch)





DIM	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00		0.05
A3		0.203 REF	
b	0.15	0.20	0.25
D		7.00 BSC	
E		7.00 BSC	
D2	5.60	5.70	5.80
E2	5.60	5.70	5.80
e		0.40 BSC	
L	0.35	0.40	0.45
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

NOTES

1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.

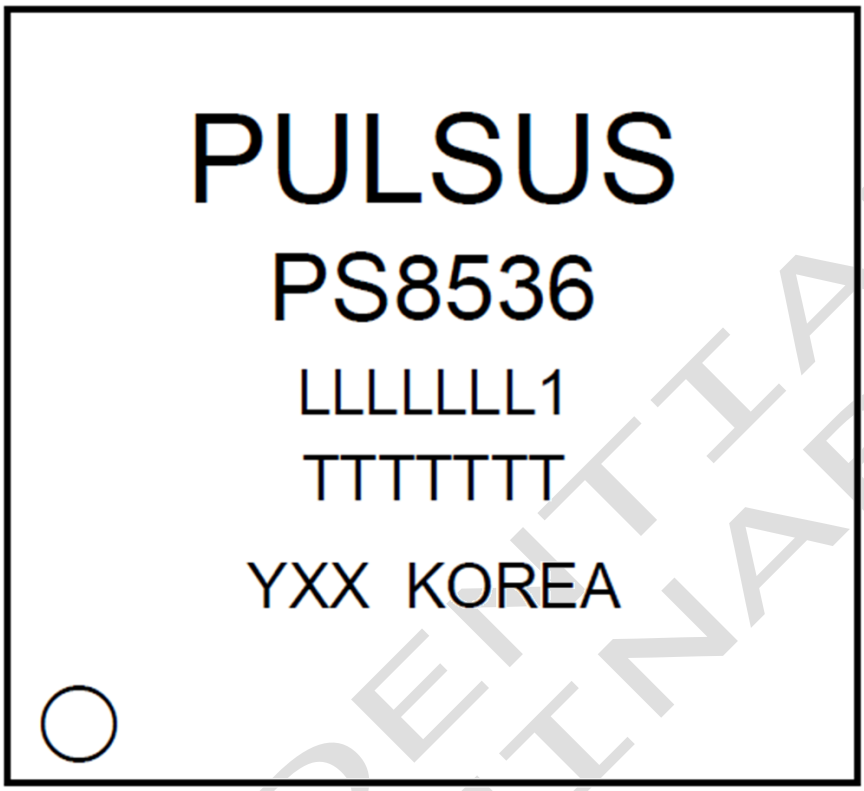
2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

3.0 DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.1mm IS ACCEPTABLE.

4.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.

5.0 RADIUS ON TERMINAL IS OPTIONAL.

3.2 Marking Information



Device marking description			
PULSUS	Chip vendor		
PS8536	Product name		
LLLLLLL	Die1 Wafer Lot #	1	Assembly Site Code
TTTTTTT	Die2 Wafer Lot #		(e.g. 1=ASE Korea)
Y	Last digit of the year assembled (e.g. 9=2009, 0=2010, 1=2011)		
XX	Work week	KOREA	Nationality of chip vendor

4 APPLICATION INFORMATION